Roberto Giorgi

Curriculum Vitæ (13 March 2018)

Date of birth	13th March 1964
Marital Status	Married – with two daughters
Languages	Italian(native), English(fluent)
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Main Facts

- Roberto Giorgi is an Associate Professor at Dept. of Information Engineering, University of Siena, Italy.
- He was Research Associate at the University of Alabama in Huntsville, USA.
- He received his PhD in Computer Engineering and his MS in Electronics Engineering, Summa cum Laude both from University of Pisa, Italy.
- Currently, he is the Coordinator of the European Project AXIOM (3.9Meuro cost, 2015-2018, 7 partners), about designing and manufacturing the next generation board for Cyber-Pysical Systems.
- He coordinated the TERAFLUX project (8.5Meuro cost, 2010-2014, 11 partners) in the area of Future and Emerging Technologies for Teradevice Computing.
- He is member of the HiPEAC Network of Excellence (High Performance Embedded-system Architecture and Compilation) since 2004.
- He was Deputy Steering Committee in the HiPEAC, Application leader in the ERA project (Embedded Reconfigurable Architectures), participated to SARC (Scalable ARChitectures) and attracted more than 3 Million Euro of Research Funding to the University of Siena in the last decade.
- He took part in ChARM project, developing software for performance evaluation of ARM-processor based embedded systems with cache memory.
- He has been IEEE Judge for the IEEE-CSIDC (Computer Society International Design Competition).
- He led the project "Bluesign Translator", which received a 5th worldwide prize by IEEE and top companies, and received the FORUM-P.A. prize by the Italian Ministry of Technological and Scientific Innovation, as absolute winner in the category of "actions for the social integration of disadvantaged people through ICT".
- He has been selected by the European Commission as an independent expert for evaluating ICT European Projects.
- He is co-author of more than 110 scientific papers.
- His current interests include Computer Architecture themes such as Embedded Systems, Multiprocessors, Memory System Performance, Workload Characterization.
- He is a Lifetime member of ACM and a Senior Member of the IEEE, IEEE Computer Society.

Contents

1 Appointments

Associate Professor of Computer Architecture (with tenure) Oct. 2006-present
University of Siena, Dept. of Information Engineering, Siena, Italy

Assistant Professor of Computer Architecture (with tenure) Mar. 1999-Sept. 2006
University of Siena, Dept. of Information Engineering, Siena, Italy

Post-Doctoral Researcher Feb. 1999-Jan. 2000
The University of Alabama in Huntsville, AL, USA

- "Experimental Research for the Evaluation of Multithreaded Architectures" (**NSF** grant #9805216)
- "Multithreading Systems" (Italian National Research Council (**CNR**) grant #203.15.9)

Visiting Scholar May 1998
University of Belgrade, Serbia, Yugoslavia
Visiting Scholar Jul. 1997-Aug.1997
University of Texas in Arlington, TX, USA
Visiting Scholar Jul. 1996-Aug.1996
University of Washington, WA, USA

2 Education

PhD in "Information Engineering: Electronics, Informatics, Telecom." Oct. 1995-Sept. 1998
University of Pisa, Pisa, Italy
"Evaluation of a Coherence Protocol for Eliminating Passive Sharing in Shared-Bus Multithreaded Multiprocessors"
Thesis advisor: Prof. Cosimo Antonio Prete

MEng in "Electronics Engineering" July 1995
University of Pisa, Pisa, Italy
"Performance Evaluation of Multiprocessor Systems, based on Real Traces Analysis"
Thesis advisor: Prof. Cosimo Antonio Prete
Mark: **Summa cum Laude** (**110/110+Laude**)

High-School Diploma "Scientific Lyceum" July 1983
Viareggio LU, Italy
Mark: **60/60**

3 Awards

- 2006(May) FORUM P.A./CNIPA Award by Italian Ministry of Innovation and Technologies for the best action to accessibility of public administration by the disable through the project "BlueSign Translator" (**absolute winner in the category**). Web sites: http://www.bluesign.it/ e https://it.wikipedia.org/wiki/Blue_Sign.
- 2002(June) IEEE Award (5th worldwide price 2000 USD) for the realization of a "Sign Language Translator" based on Bluetooth Technology for helping the Deaf in a course projects, IEEE Computer Science International Design Competition (CSIDC).
- Best paper awards for works [C61], [C42], [C2] (see below).

4 Technology Transfer

- 2014-2017 Coordinating the EU-funded Research and Innovation Action AXIOM, which realized through partner SECO an FPGA-based Italian-manufactured single computer board.
- 2007-2009 Cooperation Agreement with RAI (RADIOTELEVISIONE ITALIANA) for the implementation of advanced solutions for the integration of automatic translation systems of Sign Language for the Deaf in the television.
- 2003-2008 Cooperation with Italian Association for the Education of the Deaf (AIES, Associazione Italiana Educazione Sordi) to support the study of a multimedial system for communicating in Italian Sign Language (LIS, Lingua Italiana dei Segni).
- 1998(Nov)-1999(Jan) Contract for "Performance Evaluation of Coherence Protocols for Single-Chip Embedded Multiprocessors" at the Department of Information Engineering, University of Pisa.

- 1995(Sep)-1995(Dec) Contract for "Performance Evaluation of Multiprocessor System under Different Software Workload" at the Department of Information Engineering, University of Pisa.
- 1995(Sep)-1995(Oct) Cooperation with VLSI Tech. Inc., San Jose, CA, U.S.A. to support the realization of X/MOTIF Graphical Interface for the commercial software "ChARM - JumpStart 3.0".

5 Fields of Interest

- **Scalable and Adaptive Embedded Systems** We are entering the Cyber-Physical age, in which both objects and people will become nodes of the same digital network for exchanging information. Therefore, in our imaginary, the general expectation is that "things" or systems will become somewhat smart as people, allowing rapid and close interactions not only system-system, but also human-system, system-human. More scientifically, we expect that such Cyber-Physical Systems (CPSs) will at least react in real-time, have enough computational power for the assigned tasks, consume the least possible energy for such task (energy efficiency), scale up through modularity, allow for an easy programmability across performance scaling and exploit at best existing standards at minimal costs. The whole set of these expectations impose scientific and technological challenges that need to be properly addressed. In this line of reseach (projects AXIOM and ERA), we aim at researching new software/hardware architectures for CPSs to meet the above expectations. The technical approach aims at solving fundamental problems to enable easy programmability of multi-core multi-board systems through the open-source OmpSs programming model, leveraging Distributed Shared Memory (DSM) inspired concepts across the modules. The OmpSs will allow accelerating functions through an FPGA (Agility). In particular, to the best of our knowledge, this is the first time that DSM will be effectively demonstrated on an embedded modular system (eXtensibility). Modular scalability will be possible thanks to a fast interconnect that will enrich the module. To this aim, an innovative modular ARM-based board with enhanced capabilities for interfacing with the physical world will be designed and demonstrated in key scenarios such as Smart Video-Surveillance, Smart Living/Home (Domotic) or others [C60],[C56],[C54],[C53],[C47],[C46],[C38],[C41],[C24].
- **Architectures and Tools for Many-Core systems** Future Teradevice Systems, i.e. systems with more then 10^{12} transistors in a single package or multi-layer chip, exhibit a large amount of parallelism (e.g., general purpose 1000 cores) that is not used efficiently by current applications and programming models. The work done in this field of research regards the development of architectures that both builds on existing solutions at the architectural level and try to enable the execution of parallel programs even n the case of sequential programming models. This is made possible by exploiting a parallel generation and scheduling of threads and combining concepts of dataflow. An essential aspect becomes to be able to assess the performance of these new platforms that not yet exist, using appropriate tools [J22],[J21],[J20],[J18],[J17],[J13],[C58],[C57],[C55],[C50],[C45],[C49],[C48],[C42]. In addition, applications are becoming more complex, requiring more computational resources as they need to process larger and larger amounts of data ("big-data"); a typical examples are bioinformatics applications as we need a shorter time to analyze bilogical data and have more precise information on the health status of a patient. Processing may not necessarily be a classic data-parallel problem: in the general case of irregular applications, the effort required the programmer can be very high or even not feasible. For this reason, in this line of research we examine the methodologies that enable a more efficient execution, regardless of what the programmer specifies, by improving the hardware/software interface. The contribution in this area is a proposal for a radical change in the way applications run on the architecture, using however minimal changes to the architecture itself. The proposal is currently focusing on the use of an extended instruction set ("called T-Star", consisting of only six instructions) and its architectural support. In order to demonstrate the applicatbility to current computing systems we used the x86_64 architecture, but we analyzed the feasability also on other previous architectures such as the Cell Processor from Sony-Toshiba-IBM [C36],[C35],[C34],[C33],[C31].
- **Low-Power techniquies for Embedded Systems** One of the most critical parts of an embedded sytem is the cache memory, since it affects performance and large portions of the power consumption. In particular, the losses (leakage) continue to be a problem despite the use of new materials with high dielectric constant (Hi-K) and even in the 11nm technologie nodes and at normal operating temperatures (over 30 degrees Celsius). An innovative proposal is based on the filtering effects of a non-low-power cache stage followed by a low-power cache stage. Significant improvements can so be achieved at virtually negligible costs in terms of area and complexity [C37],[C32],[C30],[C29].
- **Design techniques for architectural support of Elliptic Curve Cryptography** The cryptographic systems based on elliptic curves (or ECC Elliptic Curve Cryptography) have the advantage to work with operands of a length of at least one order of magnitude lower than that of cryptographic standards now commonly in use, such as RSA, DSA, Diffie-Helman El-Gamal. Because of this important feature, cryptosystems based on elliptic curves are particularly suitable for use on smart cards and devices like the mobile and embedded applications. Typically, there are two possible solutions to improve the performance of ECC systems: the first is the optimization of the software, the second is the realization in hardware arithmetic coprocessors. The software implementation is certainly flexible, but the performance that would be obtained in the embedded devices are inadequate; on the contrary, hardware processing is expensive and does not offer the desired flexibility. The research carried ou, using the instruction set of ARM processors, widely used in embedded applications, show promising results. The architectural support that involves on the one hand the minimum hardware changes has been identifed. This has also other benefits in terms of reducing the execution time and the overall used resourcesi [J16],[J14],[J9],[C22],[C20].

- **Evaluation and proposal of a new microprocessor architecture based on multithreading and dataflow concepts, which enables to overcome traditional limitations of Superscalars and VLIWs** In this research work, it has been analyzed the possibility of using a new processor architecture that could improve considerably the iperformance of current architectures based mainly on the Superscalar and VLIW paradigms. This research has led to the definition of a new type of microprocessor that builds on the concepts of dataflow and expresses them fully in current multithreaded systems. The architecture is named Scheduled Data-Flow (SDF) and it has been expanded into novel models called Decoupled Threaded Architecture (DTA). Later developments led to the TERAFLUX architecture. Several generations of simulators have been developed in order to arrive lately to model a full-system 'as-is' running an off-the-shelf Linux Operating System and consisting of multiple cores (up to 32 per node have been explored) and multiple nodes. The results were very encouraging already with the first sumulated prototypes and demonstrates that this type of architecture allows not only to achieve superior performance in respect to current superscalar processors and VLIWs, but also to fully exploit the thread-level parallelism, thus overcoming the limitations of scalability of the processor internal resources (e.g., limited instruction level parallelism) of current architectures [J19],[J17],[J8],[J7],[J6],[J5],[C59],[C51],[C44],[C43],[C40],[C39],[C28],[C17],[C12].

- **Innovative solutions for cache-cherence of single-chip multiprocessor systems under thread migration** In this line of research, it has been proposed a new coherence protocol, called PSCR (Shared Passive Copy Removal), evaluated in the case of shared-bus, shared-memory multicores. This architecture is particularly attractive given its low cost and simplicity and in fact it has been adopted since the year 2000 by all major processor manufacturers. While it is necessary to introduce private cache memories in order to overcome the limitations of an excessive traffic on the shared-bus, we also need to introduce mechanisms to manage the consistency of multiple copies of the application data. This problem is exacerbated by thread migration to available cores, in turn necessary to balance the load in the machine. However, this research highligted that a considerable part of the traffic is unnecessary because it is due to copies that mistakenly appear as shared while they are actually private: this situation has been named "passive sharing". The proposed solution consist in a novel coherence protocol (PSCR) that completely eliminate the passive sharing. The evaluation of such protocol demonstrated that PSCR can achieve a higher scalability as compted to six other protocols known in the literature or widely used, such as the MESI protocol. The results showed that with the use of PSCR, multicores with more than 30 cores are feasible even with a simple and inexpensive solution such as the shared-bus interconnect [J3],[J2],[J1],[C10],[C7],[C4],[C3],[C2],[C1].

- **Study of solutions for improving performance of Web-Servers and Data-Base Management Systems (DBMS)** Web servers and DBMSs (Data Base Management Systems) are particularly critical from the point of view of performance. E.g., E-Commerce systems, OLTP systems (Online Transaction Processing) and DSSs (Decision Support System) are implemented with an N-tier distributed architecture or also simply with a three-tier architecture, in which second layer acts primarily a Web-Server and third layer acts primarily a DBMS (being the first layer consists of the client or Web browser). To cope with a high number of requests, the typical solution is to use a Network of Workstations (or Clusters). In cases where the single node constitutes per se a multicore system, it is necessary to use every possible solution to maximize performance. In particular, taking into account the organization of the system, the machine load (workload) consists of intense multitasking activity (generated by both Web client requests and DB queries) that involves a strong commitment Operating System (e.g., Scheduler, Virtual Memory) in order to obtain a balanced load. Taking this platform as a case study, we tried to highlight possible architectural solutions to improve significantly the performance of the machine. Through the combined intervention on restructuring of kernel data, operating system virtual mapping, OS scheduler and the coherence protocol, we found out that it is possible even to double the performance of a multicore system. The evaluation methodology is based on widespread benchmarks such as TPC-W and TPC-D [J12],[J11],[J10],[C21],[C19],[C16],[C15],[C14],[C13],[C11],[C9].

- **Handheld Multimedia Devices for the Deaf** Starting from the analysis of the actual needs of the Deaf, it emerged that the Deaf prefers to communicate through the sign language, because it is perceived as their mother tongue and, in fact, it allows an immediacy of communication otherwise difficult to obtain. The current developments in information technology and the increase of the processing power of portable devices (in particular smart-phones, handheld computers and other mobile devices) enabled to think about the design of assistive technology that can make an automatic translation of text into sign language for the Deaf. As the processing power and energy consumption of portable devices are anyway limited, appropriate solutions have to be explored in order to enable an acceptable usability by the Deaf Community. This research achived a working prototype that is able to translate natural language text (in this study, Italian) into Italian Sign Language (LIS). Moreover, a digital dictionary has been constructed and validated with the help of the Deaf. This dictionary extends the current state-of-the art paper dictionary by more than 20% of terms [J15],[C27],[C26],[C25],[C23].

- **Innovative cache design techniques for designing embedded systems and for computer architecture education** The processing system internals contain many details which cannot be checked directly, such the importance of pipelines or caches. Therefore, it is crucial to rely on experimental tools capable on the one hand to understand the inside of the microprocessor and the cache memory through a simple web-based interface and on the other hand to enable the teacher to monitor the student activities while he/she is exploring the complexity of the processor. In this research, new tools had been implemented. Interstingly, some of the features of those tools (such us the exploration of 3D locality curves) has been found useful also for system designer and has been included in commercial tools such as the ChARM for the VLSI Technolgy Inc. Jumpstart Kit [J4],[C52],[C18],[C8],[C6][C5].

6 Research Projects

R20. 2015-2018 Role: **Coordinator(PI)** (European Commission - H2020), "AXIOM: Agile, eXtensible, fast I/O Module for the cyber-physical era" - project id. 645496, (EUR 3'945'937 total funding, EUR **985'000** for UNISI) - Selection Mark: 14.5/15.

R19. 2015-2018 Role: **Workpackage Leader WP7 "Evaluation and Design Space Exploration"** (European Commission - H2020), "AXIOM: Agile, eXtensible, fast I/O Module for the cyber-physical era" - project id. 645496.

R18. 2012-2014 Role: **Coordinator(PI)** (European Commission - Special FP7-FET objective for cooperating with non-EU partners), Future and Emerging Technologies - Large Project - TERAFLUX–INCO "Exploiting Dataflow Parallelism in Teradevice Computing in cooperation with University of Delaware, USA" - project id. 309229, (EUR 420'000 total funding, EUR **150'000** for UNISI) - Selection Mark: 15/15.

R17. 2010-2014 Role: **Workpackage Leader WP1 "Integration activities between TERAFLUX and UD"** (European Commission - FP7-FET), Future and Emerging Technologies - Large Project - "TERAFLUX – Exploiting Dataflow Parallelism in Teradevice Computing in cooperation with University of Delaware, USA" - project id. 309229.

R16. 2010-2014 Role: **Coordinator(PI)** (European Commission - FP7-FET), TERAFLUX: "Exploiting Dataflow Parallelism in Teradevice Computing" project id. 249013, (EUR 5'700'000 total funding, EUR **1'167'000** for UNISI) - Selection Mark: 15/15.

R15. 2010-2014 Role: **Workpackage Leader WP7 "Common Simulation and Compilation Platform"** (European Commission - FP7-FET), "TERAFLUX – Exploiting Dataflow Parallelism in Teradevice Computing" project id. 249013.

R14. 2010-2013 Role: **Workpackage Leader WP1 "Embedded Application Analysis"** (European Commission - FP7-ICT), ERA: "Embedded Reconfigurable Architecture" - project id. 249059, (EUR 2'800'000 total funding, EUR **417'000** for UNISI).

R13. 2010-2014 Role: **Participation** (HiPEAC networking funding), HIPEAC3: "High-Performance Embedded Architecture and Compilation", (EUR 4'000 total funding, EUR **4'000** for UNISI).

R12. 2008-2009 Role: **Coordinator(PI)** (Monte dei Paschi di Siena Foundation), "Integration of Sign Language for the Deaf in the digital television", (EUR 50'000 total funding, EUR **50'000** for UNISI).

R11. 2007-2008 Role: **Coordinator(PI)** (Regione Toscana - through National Association of the Deaf), "Extension of the digital vocabulary of an automated Sign Language System for the Deaf", (EUR 10'000 total funding, EUR **10'000** for UNISI).

R10. 2008-2012 Role: **Participation** (HiPEAC networking funding), HiPEAC Network of Excellence HIPEAC2: "High-Performance Embedded Architecture and Compilation", (EUR 5'000 total funding, EUR **5'000** for UNISI).

R9. 2008 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), HiPEAC Network of Excellence "Multithreaded Dataflow Architectures", (EUR 10'240 total funding, EUR **10'240** for UNISI).

R8. 2008 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), "Cache implications of non-blocking thread execution in a multithreaded architecture", (EUR 14'000 total funding, EUR **14'000** for UNISI).

R7. 2005-2009 Role: **Participation** (European Commission - FP6-FET), Future and Emerging Technologies - Integrated Project (IP) SCALA/SARC: "Scalable ARChitectures", (EUR 8'500'000 total funding, EUR **(through University of Pisa) 90'000** for UNISI).

R6. 2006 Role: **Coordinator of HiPEAC research cluster** (HiPEAC seed funding), HiPEAC Network of Excellence "Scalable Multicore Architectures" in Cooperation with Universities of Goteborg-Chalmers (Sweden), Delft-TUD (Netherlands), Barcelona-UPC (Spain), (EUR 30'000 total funding, EUR **10'000** for UNISI).

R5. 2004-2008 Role: **Deputy Steering Committee** (European Commission - FP6-NoE), HiPEAC Network of Excellence "High-Performance Embedded Architecture and Compilation", coordination: Polytechnic University of Catalonia, Spain (UPC), (EUR 3'900'000 total funding, EUR **n/a** for UNISI).

R4. 2004-2005 Role: **Coordinator(PI)** (Italian Investment Fund for Basic Research (FIRB), Italian Ministry of Education, University and Research (MIUR)), "Innovative Architectures for High Performance Processors", (EUR 60'000 total funding, EUR **30'000** for UNISI).

R3. 2004 Role: **Coordinator(PI)** (Monte dei Paschi di Siena Foundation), "Study and Realization of a Multimedia System for Translating and Communicating with the Sign Language for the Deaf", (EUR 40'000 total funding, EUR **40'000** for UNISI).

R2. 2004-2005 Role: **Coordinator(PI)** (University Research Plan (PAR) of the University of Siena), "Innovative Architectures for Multimedia Applications in Embedded Systems", (EUR 15'000 total funding, EUR **15'000** for UNISI).

R1. 2003-2005 Role: **Participation** (Italian Investment Fund for Basic Research (FIRB), Italian Ministry of Education, University and Research (MIUR)), "Reconfigurable Platforms for Broadband Mobile Devices", activity of "Development of Innovative Cryptographic Techniques", coordinator prof. Enrico Martinelli, (EUR 320'000 total funding, EUR **80'000** for UNISI).

7 Journal Papers [statistics]

J30. D. Theodoropoulos, S. Mazumdar, E. Ayguade, N. Bettin, J. Bueno, S. Ermini, A. Filgueras, D. Jimenez-Gonzalez, C. Alvarez Martinez, X. Martorell, F. Montefoschi, D. Oro, D. Pnevmatikatos, A. Rizzo, P. Gai, S. Garzarella, B. Morelli, A. Pomella, R. Giorgi, "The AXIOM platform for next-generation cyber physical systems", *Microprocessors and Microsystems*, 2017, SCOPUS: 2-s2.0-85021936895, WOS:000407984000049, DOI: 10.1016/j.micpro.2017.05.018.

J29. L. Verdoscia, R. Giorgi, "A Data-Flow Soft-Core Processor for Accelerating Scientific Calculation on FPGAs", *Mathematical Problems in Engineering*, vol. 2016, no. 1, Apr. 2016, pp. 1-21, (article ID 3190234), ISSN: 1563-5147, SCOPUS: 2-s2.0-84973355670, DOI: 10.1155/2016/3190234.

J28. A. Rizzo, G. Burresi, F. Montefoschi, M. Caporali, R. Giorgi, "Making IoT with UDOO", *Interaction Design and Architecture(s)*, vol. 1, no. 30, Dec. 2016, pp. 95-112, ISSN: 1826-9745, SCOPUS: 2-s2.0-85007362581, WOS:000393571700007.

J27. C. Alvarez, E. Ayguade, J. Bosch, J. Bueno, A. Cherkashin, A. Filgueras, D. Jiminez-Gonzalez, X. Martorell, N. Navarro, M. Vidal, D. Theodoropoulos, D. Pnevmatikatos, D. Catani, D. Oro, C. Fernandez, C. Segura, J. Rodriguez, J. Hernando, C. Scordino, P. Gai, P. Passera, A. Pomella, N. Bettin, A. Rizzo, R. Giorgi, "The AXIOM Software Layers", ***ELSEVIER Microprocessors and Microsystems***, vol. 47, Part B, 2016, pp. 262-277, ISSN: 0141-9331, SCOPUS: 2-s2.0-84979544372, WOS:000390513300003, DOI: 10.1016/j.micpro.2016.07.002.

J26. S. Weis, A. Garbade, B. Fechner, A. Mendelson, R. Giorgi, T. Ungerer, "Architectural Support for Fault Tolerance in a Teradevice Dataflow System", ***Springer Int.l Journal of Parallel Programming***, New York, NY, USA, vol. 44, no. 2, Apr 2016, pp. 208-232, ISSN: 1573-7640, SCOPUS: 2-s2.0-84901582160, WOS:000373569600002, DOI: 10.1007/s10766-014-0312-y.

J25. R. Giorgi, S. Mazumdar, S. Viola, P. Gai, S. Garzarella, B. Morelli, D. Pnevmatikatos, D. Theodoropoulos, C. Alvarez, E. Ayguade, J. Bueno, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, "Modeling Multi-Board Communication in the AXIOM Cyber-Physical System", *Ada User Journal*, vol. 37, no. 4, December 2016, pp. 228-235, ISSN: 1381-6551, SCOPUS: 2-s2.0-85004143304.

J24. P. Burgio, C. Alvarez, E. Ayguade, A. Filgueras, D. Jimenez-Gonzalez, X. Martorell, N. Navarro, R. Giorgi, "Simulating next-generation cyber-physical computing platforms", *Ada User Journal*, vol. 37, no. 1, Mar. 2016, pp. 59-63ISSN: 1381-6551, SCOPUS: 2-s2.0-84974555745.

J23. S. Wesner, L. Schubert, R. Badia, A. Rubio, P. Paolucci, R. Giorgi, "Special Section on Terascale Computing", ***ELSEVIER Future Generation Computer Systems***, New York, NY, USA, vol. 53, July 2015, pp. 88-89, SCOPUS: 2-s2.0-84939190506, WOS:000361075400008, DOI: 10.1016/j.future.2015.07.015.

J22. R. Giorgi, A. Scionti, "A scalable thread scheduling co-processor based on data-flow principles", ***ELSEVIER Future Generation Computer Systems***, Amsterdam, Netherlands, vol. 53, Dec. 2015, pp. 100-108, ISSN: 0167-739X, SCOPUS: 2-s2.0-84939202928, WOS:000361075400010, DOI: 10.1016/j.future.2014.12.014.

J21. R. Giorgi, "Transactional Memory on a Dataflow Architecture for Accelerating Haskell", *WSEAS Trans. Computers*, vol. 14, 2015, pp. 546-558, ISSN: 1109-2750.

J20. P. Burgio, C. Alvarez, E. Ayguadé, A. Filgueras, D. Jiménez-González, X. Martorell, N. Navarro, R. Giorgi, "Simulating next-generation Cyber-physical computing platforms", *Ada User Journal*, vol. 36, no. 4, Dec. 2015, pp. 259-263, ISSN: 1381-6551, SCOPUS: 2-s2.0-84960085502.

J19. R. Giorgi, R. Badia, F. Bodin, A. Cohen, P. Evripidou, P. Faraboschi, B. Fechner, G. Gao, A. Garbade, R. Gayatri, S. Girbal, D. Goodman, B. Khan, S. Koliaï, J. Landwehr, N. Minh, F. Li, M. Lujàn, A. Mendelson, L. Morin, N. Navarro, T. Patejko, A. Pop, P. Trancoso, T. Ungerer, I. Watson, S. Weis, S. Zuckerman, M. Valero, "TERAFLUX: Harnessing dataflow in next generation teradevices", ***ELSEVIER Microprocessors and Microsystems***, Netherlands, Amsterdam, vol. 38, no. 8, Part B, 2014, pp. 976-990, ISBN: N/A, ISSN: 0141-9331, SCOPUS: 2-s2.0-84912558447, WOS:000347755500013, DOI: 10.1016/j.micpro.2014.04.001.

J18. A. Portero, Z. Yu, R. Giorgi, "TERAFLUX: Exploiting Tera-device Computing Challenges", ***ELSEVIER Procedia Computer Science***, New York, NY, USA, vol. 7, 2011, pp. 146-147, (Proc. 2nd European Future Technologies Conf. and Exhibition 2011 (FET 11)), ISBN: N/A, ISSN: 1877-0509, SCOPUS: 2-s2.0-84856501660, WOS:000299100900045, DOI: 10.1016/j.procs.2011.09.081.

J17. S. Bartolini, I. Branovic, R. Giorgi, E. Martinelli, "Effects of Instruction-set Extensions on an Embedded Processor: a Case Study on Elliptic Curve Cryptography over GF(2/sup m/)", ***IEEE Trans. Computers***, Los Alamitos, CA, USA, vol. 57, no. 5, May 2008, pp. 672-685, ISBN: N/A, ISSN: 0018-9340, SCOPUS: 2-s2.0-64349109200, WOS:000254054500008, DOI: 10.1109/TC.2007.70832.

J16. S. Bartolini, P. Bennati, R. Giorgi, "L'Informatica per i sordi: su palmare la lingua dei segni", *Mondo Digitale*, June 2007, pp. 42-49, ISSN: 1720898X, SCOPUS: 2-s2.0-34547978230.

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12 Technical Reports and Deliverables

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13 Intellectual Property

IP2. S. Bartolini, P. Bennati, R. Giorgi, "BlueSign 2", *SIAE 24-02-2006/001*, Reg. 24 Feb. 2006.

IP1. P. Bennati, T. Capasso, V. Di Massa, F. Giallombardo, R. Giorgi, M. Guerrini, E. Maggio, N. Nannetti, "BlueSign Translator", *SIAE 002568, Ord. D003454*, Reg. 21 Mar. 2003.

14 Educational and Research Software

SW7. 2013(Sep) The Dataflow Run Time (DRT) http://sourceforge.net/projects/drt/

- A runtime library to code and debug programs that are based on a Thread-Level-Parallelism Instruction Set Extension (TLP ISE).

SW6. 2013(Jun) COTSon Thread Scheduler Unit (TSU) http://sourceforge.net/p/cotson/code/HEAD/tree/branches/timing-unisi/tsu4/

- A functional and timing model for an x86_64 based full-system. It uses a custom Instruction Set Extension (ISE) to support a dataflow based execution model. The model is a plugin of the HP-Labs COTSon full-system simulator.

SW5. 2009(May) FREESS: The Free SuperScalar simulator http://www.dii.unisi.it/ giorgi/freess

- Simulates a simple Superscalar processor step-by-step, visualizing the activity of renaming, instruction window, reorder buffer, load/store queues.

SW4. 2010(Jun) The ERA BENCHMARK-SUITE http://www.dii.unisi.it/ giorgi/ebs

- A banchmark suite for research on embedded system for mobile.

SW3. 2004(May)The WEBMIPS: Web-based MIPS simulator http://www.dii.unisi.it/ giorgi/WEBMIPS

- Simulates a MIPS pipeline inside a web browser. The architectural elements are visualized while instructions pass through the pipeline.

SW2. 2003(Sep) The BASICRYPT BENCHMARK-SUITE http://www.dii.unisi.it/ giorgi/basicrypt

- A banchmark suite for research on Elliptic Curve Cryptograpy.

SW1. 2003(June) JCACHESIM cache+cpu web-based simulator http://www.dii.unisi.it/ giorgi/jcachesim

- Simulates a cache memory and its internal operation, while executing simple MIPS programs. It runs in a java enabled web browser.

15 Public Talks

T38. 2018(Jan), (SHiP-CPS: Software-Hardware Platforms for Syber-Pysical Systems), "The AXIOM platform for Cyber-Physical Systems" (presentation)

T37. 2017(Sep), (Second Italian Workshop on Embedded Systems), "The AXIOM-board: bringing programmability, acceleration, scalability into a 64-bit hand-size board" (presentation)

T36. 2016(Sep), (First Italian Workshop on Embedded Systems), "AXIOM: A 64-bit scalable embedded system including Arduino socket and on-chip FPGA" (presentation)

T35. 2016(Sep), (VIMAR, Marostica, Italy), "AXIOM Operating System analysis" (presentation)

T34. 2016(Jun), (Barcelona Supercomputing Center, Barcelona, Spain), "AXIOM Design Exploration Tools" (presentation)

T33. 2016(Apr), (ARTEMIS Spring Event, Vienna, Austria), "The AXIOM Cyber Ohysical System" (presentation)

T32. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), "The AXIOM project" (presentation)

T31. 2015(May), (Barcelona Supercomputing Center, Barcelona, Spain), "The COTSon simulation environment" (tutorial)

T30. 2015(Feb), (CEA conference, Dubai, UAE), "Accelerating Haskell on a Dataflow Architecture: a case study including Transactional Memory"

T29. 2014(Oct), (MPP Workshop, Paris, France), "An Introduction to DF-Threads and their Execution Model"

T28. 2014(Sep), (Istituto di Calcolo ad Alte Prestazioni, Napoli, Italy), "TERAFLUX: Harnessing 1 TERA devices in a single package"

T27. 2013(Aug), (Georgia Tech, Atlanta, GA, USA), "TERAFLUX overview and the T* instruction extension"

T26. 2013(Aug), (University of Delaware, DE, USA), "TERAFLUX Research Overview"

T25. 2013(Oct), (SoC conference,Tampere,FI), "The TERAFLUX Project OVERVIEW" (presentation)

T24. 2013(Oct), (SoC conference,Tampere,FI), "MANY-CORE CHIPShe New High-Performance Computing Platfoms: Hardware Thread-Level Parallelism Support in Many-Core Architectures" (tutorial)

T23. 2013(Jun), (CASTNESS workshop, Barcelona, Spain), "The T* Instruction Set Extension" (presentation)

T22. 2013(May), (University of Pisa, Italy), "DATAFLOW: different answer to achieve Scalabilty" (tutorial)

T21. 2013(Mar), (DATE Conference, Grenoble, France), "Lessons learnt from European Projects" (Panel)

T20. 2013(Feb), (University of Siena, Italy), "Creation and Managementf a Large Scale search Project"

T19. 2012(Jun), (), "TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices"

T18. 2012(May), (Computing Frontiers conference, Cagliari, Italy), "TERAFLUX: Exploiting Dataflow Parallelism Teradevice Computing"

T17. 2012(Jun), (CASTNESS workshop, Paris, France), "TERAFLUX, Effective Operation of Dataflow Parallelism in Teradevices"

T16. 2011(Oct), (DFM Workshop, Galveston, TX, USA), "Data Flow Execution models" (panelist)

T15. 2011(Apr), (ODES workshop, CGO Conference, Chamonix, France), "TERAFLUX: exploiting DATAFLOW parallelism" (Keynote speech)

T14. 2011(Jan), (CASTNESS workshop, Rome, Italy), "Overview of a TERAFLUX-like Architecture"

T13. 2010(Jun), (International Forum on Multicores), "Integrating multicore research and the COTSon simulation platform"

T12. 2010(May), (HiPEAC Computing Week, Edinburgh UK), "TERAFLUX: exploiting DATAFLOW parallelism"

T11. 2005(May), (Dept. of Electronics and Information Systems, Ghent, Belgium), "Tiled Architectures for Embedded Systems"

T10. 2004(Oct), (Dept. of Computer Engineering, Delft, Olanda), "Non- Conventional Microprocessor Architectures"

T9. 2004(Sep), (HiPEAC Workshop, Juan les Pins, France), "Embedded-System Research Overview"

T8. 2003(Nov), (University of Pisa, Italy), "Non-Convential Microprocessor Architectures"

T7. 2002(Jan), (SSGRRw-2002 Conference, L'Aquila, Italy), "Non-Convential Microprocessor Architectures"

T6. 2001(Nov), (SGS-Thomson Advanced Research Laboratory, Milan, Italy), "Architetture Non-Convenzionali per Microprocessore"

T5. 2000(Apr), (University of Siena, Italy), "Introduzione alla Architettura Scheduled Data-Flow -SDF"

T4. 1999(May), (Dept. of Electrical and Computer Engineering, University of Alabama in Huntsville, AL, USA), "Scheduled Dataflow Architecture: problems and issues"

T3. 1998(May), (University of Belgrade, Serbia, Yugoslavia), "Simulating Composite Workloads on Shared-Bus Symmetric Multiprocessors"

T2. 1997(Sep), (Facolta' di Ingegneria, Università di Salerno, Benevento), "Trace Factory: a Hybrid Approach to Trace Generation for Performance Evaluation of Shared Bus Multiprocessors"

T1. 1997(Aug), (Computer Science and Engineering Dept., University of Texas at Arlington, TX, USA), "Trace Driven Simulation of Shared-Bus Multiprocessors"

16 Supervised Collaborators/Students

1. Visting Professor
   - 2012(Sep)-2014(May) Bruce Jacob (University of Maryland)
2. Researchers
   - 2012(Apr)-2014(Jan) Alberto Scionti
   - 2012(Apr)-2013(Apr) Marco Solinas
3. Postdocs
   - 2010(Jun)-2013(Jul) Antonio Portero
   - 2012(Mar)-2013(Oct) Stamatis Kavvadias
   - 2010(Jun)-2012(Jan) Yu Zhibin
   - 2011(Sep)-2011(Dec) Sylvain Collange
   - 2010(Jun)-2011(May) Rania Mameesh
   - 2010(Jan)-2011(Jan) Vincenzo Di Massa
   - 2010(Jan)-2011(Jan) Nikola Puzovic
   - 2010(Apr)-2010(Jun) Andrea Casaccino
   - 2007(Oct)-2008(Nov) Paolo Bennati
4. Ph.D. Students
   - 2016(Oct)-present Tutoring of Ph.D. student Marco Procaccini, ciclo XXXII.
   - 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Nikola Puzovic, ciclo XXI - Thesis title: "Implementing fine/medium grained TLP support in multi-core architectures"
   - 2005(Nov)-2008(Nov) Tutoring of Ph.D. student Zdravko Popovic, ciclo XXI - Thesis title: "Multithreaded Dataflow in Tiled Architectures"
   - 2004(Nov)-2007(Sep) Tutoring of Ph.D. student Paolo Bennati, ciclo XX - Thesis title: "Embedded Systems: Low-Power techniques and applications"
   - 2001(Nov)-2005(Apr) Co-Tutoring of Ph.D. Student Irina Branovic - Thesis title: "Architectural Support for Elliptic Curve Cryptography (ECC) "
5. Graduate Students
   - 2016(Dec)-2017(Feb) Hosting of Ph.D. student Arthur Lorenzon, from UFRGS, Brazil - sponsored by a 3-month HiPEAC (H2020) mobility grant.

- 2014(Nov)-2015(Oct) Tutoring of Ph.D. student Nitin Satpute, ciclo XXX.
- 2012(Jan)-2014(Nov) Tutoring of Ph.D. student Cai Kang, ciclo XXVII.
- 2014(Aug)-2014(Nov) Tutoring of student Amit Fuchs
- 2013(Jul)-2014(Mar) Tutoring of student Haileyesus Kifle
- 2013(Nov)-2014(Mar) Tutoring of student Daniele Colobraro
- 2013(Apr)-2014(Jan) Tutoring of student Bogdan Azaric
- 2012(Jun)-2012(Nov) Tutoring of student Eliana Sala Mariet
- 2012(Jun)-2013(Aug) Tutoring of student Andrea Mondelli
- 2012(Jan)-2013(Apr) Tutoring of student Ho Nam
- 2010(Jul)-2011(Jan) Tutoring of student Caroline Concatto
- 2008(Sep)-2009(Jun) Tutoring of student Andrea Righi
- 2008(Feb)-2008(Sep) Tutoring of student Nenad Korolija
- 2008(Feb)-2008(Sep) Tutoring of student Roberto D'Aprile
- 2004(Sep)-2005(Oct) Tutoring of student Zdravko Popovic
- Orientation Activity for potential students coming from High School.
- Tutor for several Master Thesis, Faculty of Engineering, University of Siena.

6. Master Students
   - 2015 Ettore Chimenti (Bachelor), "Porting di un sistema operativo GNU/Linux su Single-board computer ARM".
   - 2007 Giovanni Burresi (Bachelor), "Valutazione delle prestazioni di IBM Cell Processor nelle simulazioni finanziarie".
   - 2005 Fabio Antonio Cassini (Master), "Realizzazione del modulo aggiuntivo per un concentratore seriale su interfacce I^2C BUS e 1-wire bus".
   - 2005 Gian Lorenzo Meocci (Bachelor), "Studio e implementazione di un sistema embedded adibito al controllo del traffico".
   - 2004 Mauro Marchetti (Master), "Realizzazione di un sistema di supporto alle decisioni per investimenti in borsa basato su analisi tecnica e analisi delle notizie".
   - 2004 Christos Ververidis (Master), "Analisi delle prestazioni di sistemi di elaborazione con cache: uno strumento visuale".
   - 2001 Lorenzo Menconi (Master), "Progettazione di un sistema di supporto alle decisioni per l'investimento finanziario" (co-advisor).

17 Professional Activities

1. Founded initiatives
   - 2017 Founding member of the IEEE Special Technical Community "Parallel Model & System: Dataflow and beyond"

2. Project Evaluator
   - Independent Expert of the European Commission for the evaluation of CHIST-ERA (Future and Emerging Technology) 2012 - FP7 (7th Framework Programme) March 2012.
   - Independent Expert of the European Commission for the evaluation of Call FET (Future and Emerging Technology) 2008 - FP7 (7th Framework Programme) Massive ICT. FP6 IST-FET-26825 SHAPES (Scalable Software Hardware Architecture Platform for Embedded Systems), November 2006 through January 2010.
   - Reviewer of NWO Projects (Netherlands Research Organization) and EU projects.
   - Consultant for the EU Call Objective ICT-2009.8.1: FET proactive 1: Concurrent Tera-device Computing, Brussels, Nov. 2008.
   - IEEE Judge (among the 8 coming from the Industry and the Academy) for IEEE Computer Science International Design Competition (CSIDC) 2001 (http://computer.org/csidc) sponsored by Intel, Toshiba, Ericsson, AMD, Microsoft, Lucent, EMC, Hewlett-Packard, Sun, Motorola, to assign prizes for 70'000 USD. June-July 2001.

3. Member of Ph.D. Graduation Committees
   - PhD External Evaluator:Universitat Politecnica de Valencia, Valencia, Spain, December 2016.
   - PhD Committe:Universitat Politecnica de Valencia, Valencia, Spain, December 2014.

- PhD Committe:Universitat Politecnica de Catalunya, Barcelona, Spain, May 2014.
- PhD Committe:Universitat Politecnica de Catalunya, Barcelona, Spain, September 2011.
- PhD Committe:Chalmers University, Goteborg, Sweeden, June 2011.
- PhD Committe:Universitat Politecnica de Catalunya, Barcelona, Spain, December 2009.
- PhD Committe:IMT - Institute for Advanced Studies, Lucca, Italy, July 2009.

4. Member of Ph.D. Selection Committees
   - University of Florence, University of Pisa, University of Siena, "Smart Computing", Sept. 2015.
   - University of Siena, Dept. of Information Engineering, Sept. 2010.
   - University of Siena, Dept. of Information Engineering, Sept. 2008.

5. Journal Editorial Boards
   - 2017(Mar)-present Associate Editor of the International Journal of Embedded Systems (IJES).
   - 2014(Jan)-present Member of the editorial board of the International Journal of Embedded Systems (IJES).
   - Co-Guest Editor of ACM Computer Architecture News (official Newsletter of ACM Special Interest Group on Computer Architecture), number of December 2001, with emphasis on Compilation Techniques, Parallel Architectures and Frontiers Topics.
   - Guest Editor of IEEE-TCCA NEWSLETTER (official Newsletter of IEEE Special Interest Group in Computer Architecture), number of January 2001, with emphasis on MEmory DEcopupled Architectures in modern microprocessors.
   - Co-Guest Editor of Journal of Embedded Computing, 2006 special issue on Embedded Single-Chip Multicore Architectures and related research - from System Design to Application Support.
   - Journal Reviewer: IEEE Transaction on Computers, IEEE Transaction on Parallel and Distributed Systems, IEEE Micro, IEEE Concurrency, Computer Journal, Journal of System Architecture, IEEE Transaction on Circuits and Systems, Elsevier Microprocessor and Microsystems, ACM Transactions on Architecture and Code Optimization (TACO).

6. Keynote Speaker
   - **Keynote Speaker**: IEEE MECO Conference 2017, Bar, Montenegro, June 2017.
   - **Keynote Speaker**: SSGRR 2002w International Conference, L'Aquila, Italy, January 2002.

7. Chairing
   - **Program Chair**: Software/Hardware platforms for Cyber-Physical Systems Workshop, Manchester, UK, January 2018.
   - **General Chair**: ACM Computing Frontiers 2017, Siena, Italy, May 2017.
   - **European-Project Program Chair**: DATE 2016, Dresden, Germany, MArch 2016.
   - **General Chair**: CASTNESS 2012, Paris, France, January 2012.
   - **General Co-Chair**: HiPEAC WRC 2011, Heraklion, Greece, January 2011.
   - **Program Co-Chair**: HiPEAC WRC 2010, Pisa, Italy, January 2010.
   - Publicity Chair: HiPEAC 2010, Pisa, Italy, January 2010.
   - Financial/Local Co-Chair: WAIFI-2008 Workshop, Siena, Italy, July 2008.
   - **Program Co-Chair**: ESA-05 Conference, Las Vegas, Nevada, USA, June 2005.
   - **General Chair**: MEDEA-2001 Workshop, Barcelona, Spain (EU), September 2001
   - **Program Chair**: MEDEA-2000 Workshop, Philadelphia, Pennsylvania (USA), October 2000
   - **General Chair and Founder**: MEDEA-2000 Workshop, Philadelphia, Pennsylvania (USA), October 2000

8. Program Committee Membership

   PC103. FPL-2018, Dublin, Ireland, August 2018.

   PC102. EUROMICRO DSD-2018, Prague, Czech Republic, August 2018.

   PC101. ScalCom-2018, Guangzhou, China, August 2018.

   PC100. Applied Reconfigurable Computing, ARC 2018, Santorini, May 2018.

   PC99. ACM SAC-2018 Special Track, Pau, France, April 2018.

   PC98. Architecture of Computing Systems, ARCS 2018, Braunschweig, Germany, April 2018.

   PC97. HiPEAC RAPIDO 2018, Manchester, Manchester, UK, January 2018.

   PC96. HiPEAC WRC WRC 2018, Manchester, UK, January 2018.

PC95. IEEE ReConFig 2017, Cancun, Mexico, December 2017.

PC94. SBACPAD-2017, Campinas, Brazil, October 2017.

PC93. IEEE FPL-2017, Ghent, Belgium, September 2017.

PC92. ICPP Embedded Multicore Systems, EMS 2017, Bristol, UK, August 2017.

PC91. IEEE MSPDS 2017, Genova, Italy, July 2017.

PC90. ACM SAC-2017 Special Track, Marrakesh, Morocco, April 2017.

PC89. Applied Reconfigurable Computing, ARC 2017, Delft, Netherlands, April 2017.

PC88. Architecture of Computing Systems, ARCS 2017, Vienna, Austria, April 2017.

PC87. HiPEAC Embedded 2017, Nurnbergm, February 2017.

PC86. HiPEAC RAPIDO 2017, Stockholm, Sweden, January 2017.

PC85. HiPEAC WRC WRC 2017, Stockholm, Sweden, January 2017.

PC84. ICPP Embedded Multicore Systems, EMS 2016, Philadelphia, PA, USA, August 2016.

PC83. IEEE ReConFig 2016, Cancun, Mexico, November 2016.

PC82. IEEE DFM-2016, Haifa, Israel, September 2016.

PC81. IEEE FPL-2016, Lausanne, Switzerland, August 2016.

PC80. ACM SAC-2016 Special Track, Pisa, Italy, April 2016

PC79. IEEE MSPDS 2016, Innsbruck, Austria, July 2016.

PC78. Architecture of Computing Systems, ARCS 2016, Nurnberg, April, 2016.

PC77. HiPEAC WRC 2016, Prague, Czech Republic, January 2016.

PC76. HiPEAC RAPIDO 2016, Prague, Czech Republic, January 2016.

PC75. IEEE DFM-2015, San Francisco, CA, USA, October 2015.

PC74. IEEE ICCD-2015, New York, USA, October 2015.

PC73. IEEE FPL-2015, London, UK, September 2015.

PC72. IEEE WCS-IOT 2015, London, UK, September 2015.

PC71. EUROMICRO DSD-2015, Funchal, Madeira, Portugal, August 2015.

PC70. IEEE M2A2-2015, New York, USA, August 2015.

PC69. WRC-2015 Workshop, Amsterdam, Netherlands, January 2015.

PC68. MULTIPROG-2015 Workshop, Amsterdam, Netherlands, January 2015.

PC67. ARCS-2015, Porto, Portugal, March 2015.

PC66. ACM SAC-2015 Special Track, Salamanca, Spain, April 2015.

PC65. IEEE ICPADS-2014, Hsinchu, Taiwan, December 2014.

PC64. IEEE ICCD-2014, Seoul, Korea, October 2014.

PC63. IEEE FPL-2014, Munich, Germany, September 2014.

PC62. IEEE DFM-2014, Edmonton (Alberta), Canada, August 2014.

PC61. IEEE M2A2-2014, Paris, France, August 2014.

PC60. 2014 ACM International Conference on Supercomputing (ICS), (External Review Committee), Munich, Germany, June 2014.

PC59. ACM SAC-2014 Special Track, Gyeongiu, South Korea, March 2014.

PC58. ARCS-2014, Lubeck, Germany, February 2014.

PC57. MULTIPROG-2014 Workshop, Vienna, Austria, January 2014.

PC56. IEEE ICPADS-2013, Seoul, Korea, December 2013.

PC55. IEEE ICCD-2013, Asheville, NC, USA, October 2013.

PC54. IEEE DFM-2013, Edinburgh, UK, September 2013.

PC53. IEEE FPL-2013, Porto, Portugal, August 2013.

PC52. IEEE M2A2-2013, Melbourne, Australia, July 2013.

PC51. HiPEAC WRC 2013, Berlin, Germany, January 2013.

PC50. ACM SAC-2013 Special Track, Trento, Italy, March 2013.

PC49. ARCS-2013, Prague, Czech Republic, February 2013.

PC48. MULTIPROG-2013 Workshop, Berlin, Germany, January 2013.

PC47. IEEE FPL-2012, Oslo, Norway, August 2012.

PC46. IEEE M2A2-2012 Workshop IEEE International Workshop on Multicore and Multithreaded Architectures and Algorithms, Madrid, Spain, July 2012.

PC45. IEEE ICCD-2012, Montreal, Quebec, Canada, September 2012.

PC44. Workshop on the Growing Problems with Scalable Heterogeneous Infrastructures (GSHI'12), Madrid, Spain, July 2012.

PC43. HiPEAC WRC 2012, Paris, France, January 2012.

PC42. ACM SAC-2012 Special Track, Trento, Italy, March 2012.

PC41. ARCS-2012, Munich, Germany, February 2012.

PC40. MULTIPROG-2012 Workshop, Paris, France, January 2012.

PC39. IEEE SEC-2011, Sydney, Australia, December 2011.

PC38. IEEE ICCD-2011, Amherst, MA, USA, October 2011.

PC37. IEEE FPL-2011, Chania, Greece, September 2011.

PC36. ACM SAC-2011 Special Track, TaiChung, Taiwan, March 2011.

PC35. ARCS-2011, Lake Como, Italy, February 2011.

PC34. MULTIPROG-2011 Workshop, Heraklion, Greece, January 2011.

PC33. IEEE ICCD-2010, Amsterdam, Netherlands, October 2010.

PC32. IEEE FPL-2010, Milano, Italy, August 2010.

PC31. MULTIPROG-2010 Workshop, Pisa, Italy, January 2010.

PC30. ACM SAC-2010 Special Track, Sierre, Switzerland, March 2010.

PC29. IEEE ICCD-2009, Lake Tahoe, California (USA), October 2009.

PC28. WoRMES 2009, Vancouver, Canada, August 2009.

PC27. ICPP 2009, Vienna, Austria, September 2009.

PC26. Computing Frontiers 2009, Ischia, Italy, May 2009.

PC25. ACM SAC-2009 Special Track, Honolulu, Hawaii (USA), March 2009.

PC24. MULTIPROG-2009 Workshop, Paphos, Cyprus, January 2009.

PC23. IEEE ICCD-2008, Lake Tahoe, California (USA), October 2008.

PC22. MEDEA-2008 Workshop, Toronto, Canada, October 2008.

PC21. IEEE SEC-2008, Beijing, China, October 2008.

PC20. MEDEA-2008 Workshop, Toronto, Canada, October 2008.

PC19. IEEE SEC-2008, Beijing, China, October 2008.

PC18. ACM SAC-2008 Special Track, Fortaleza, Brazil, March 2008.

PC17. MULTIPROG-2008 Workshop, Goteborg, Sweden, January 2008.

PC16. MEDEA-2007 Workshop, Brasov, Romania, September 2007.

PC15. HiPEAC 2007 Conference , Ghent, Belgium, January 2007.

PC14. ACM SAC-2007 Special Track, Seoul, Korea, March 2007.

PC13. MEDEA-2006 Workshop, Seattle, Washington, USA, September 2006.

PC12. ACM SAC-2006 Special Track, Dijon, France, April 2006.

PC11. HiPEAC 2005 Conference , Barcelona, Spain, November 2005.

PC10. MEDEA-2005 Workshop, Saint Loius, Missouri, USA, September 2005.

PC9. SCOPES-2005 Workshop, Dallas, Texas, USA, September 2005.

PC8. PDES-05 IEEE/IFIP Workshop, Fukuoka, Japan, July 2005.

PC7. ACM SAC-2005 Special Track, Santa Fe, New Mexico, USA, March 2005.

PC6. MEDEA-2004 Workshop, Antibes Juan-les-Pins, France, September 2004.

PC5. ACM SAC-2004 Special Track, Nycosia, CIPRO, March 2004.

PC4. MEDEA-2003 Workshop, New Orleans, Louisiana (USA), September 2003.

PC3. ACM SAC-2003 Special Track, Melbourne, Florida (USA), March 2003.

PC2. PACT-2002 Conference, Charlottesville, Virginia (USA), September 2002.

PC1. MEDEA-2002 Workshop, Charlottesville, Virginia (USA), September 2002.

18 Major Departmental Committees

- 2006 **President** of the Self-Evaluation Committee (RAV) for the Information Engineering Laurea.
- 2015(Jun)-present Member of Ph.D. Committee "Smart Computing" (Uni. of Florence, Pisa, Siena)
- 2014 Student Tutoring Committee for the University of Siena
- 2012(Nov) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2012-present Member of Department Committee for the Management of Scientific spaces.
- 2010-present Member of Admission Committee to the Master Degrees.
- 2000-present President and member of several selection procedure for Ph.D. grants (2 times), Postdoc grants (5+ times), Post-laurea grants (5+ times).
- 2002-2010 Member of Ph.D. Committee (Department of Information Engineering, Siena).
- 2001-2010 Member of Local Area Network Management (Department Information Engineering, Siena).
- 2006-2009 Member of the Evaluation Board for Master and Bachelor Degree in Computer Engineering (Faculty of Engineering, Siena).
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2001-2009 Member of the Evaluation Board for Master in New Technologies and Company Management (University of Siena).
- 2005(Oct) Member of Commission for ING-INF/05 (Computer Systems) selection call for researchers.
- 2001-2005 Member of Orientation and Tutoring Commission.
- 2001-2005 Member of the Orientation and Tutoring commission.
- 2000-2005 Design and Maintenance of Orientation WEB Site, Faculty Engineering, Siena (www.ing.unisi.it/orientamento - www.ing.unisi.it/orientamento/initinere - www.ing.unisi.it/orientaing).

19 Teaching

The following courses have been taught at the University of Siena at the School of Engineering, at the School of Economics and at the S.Chiara College.i From year 2000 until now, more than 300 ECTS credits[1] have been taught (corresponding to an average of about 18 credits per year).

As Associate Professor:

Year	Course	ECTS credits	Level	School	Language
2017-2018	Advanced Computer Architecture	9	Master	Information Engineering	English
2017-2018	Computer Architecture	6	Bachelor	Information Engineering	Italian
2016-2017	Advanced Computer Architecture	9	Master	Information Engineering	English
2016-2017	Computer Architecture	6	Bachelor	Information Engineering	Italian
2015-2016	Advanced Computer Architecture	9	Master	Information Engineering	English
2015-2016	Computer Architecture	6	Bachelor	Information Engineering	Italian
2014-2015	Advanced Computer Architecture	9	Master	Information Engineering	English
2013-2014	Advanced Computer Architecture	9	Master	Information Engineering	English
2013-2014	Computer Architecture	6	Bachelor	Information Engineering	Italian
2012-2013	Advanced Computer Architecture	9	Master	Information Engineering	English
2012-2013	Computer Architecture	6	Bachelor	Information Engineering	Italian
2011-2012	Advanced Computer Architecture	9	Master	Information Engineering	Italian
2011-2012	Computer Architecture	6	Bachelor	Information Engineering	Italian
2010-2011	Advanced Computer Architecture	9	Master	Information Engineering	Italian
2010-2011	Computer Architecture	6	Bachelor	Information Engineering	Italian
2009-2010	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2009-2010	Computer Architecture	6	Bachelor	Information Engineering	Italian
2008-2009	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2008-2009	Computer Architecture	6	Bachelor	Information Engineering	Italian

[1] One ECTS credit corresponds to about 10 hours of teaching and 15 additional hours of personal study the student.

2007-2008	Low Power Architectures	2	Ph.D.	Information Engineering	Italian
2007-2008	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2007-2008	Information Security	3	Master	Management of Financial Inst.	Italian
2007-2008	Computer Architecture	6	Bachelor	Information Engineering	Italian
2006-2007	Low Power Architectures	2	Ph.D.	Information Engineering	Italian
2006-2007	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2006-2007	Information Security	3	Master	Management of Financial Inst.	Italian
2006-2007	Computer Architecture	6	Bachelor	Information Engineering	Italian
2005-2006	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2005-2006	Information Security	3	Master	Management of Financial Inst.	Italian
2005-2006	Computer Architecture	6	Bachelor	Information Engineering	Italian

As Assistant Professor:

Year	Course	ECTS credits	Level	School	Language
2004-2005	Advanced Computer Architecture	6	Master	Information Engineering	Italian
2004-2005	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2004-2005	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2003-2004	C++ Programming Laboratory	2	Master	Information Engineering	Italian
2003-2004	Programming Fundamentals	3	Master	Digital Economy end E-business	Italian
2003-2004	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2003-2004	Computer Architecture	6	Bachelor	Information Engineering	Italian
2003-2004	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2002-2003	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2002-2003	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2002-2003	Programming Fundamentals	3	Master	Digital Economy end E-business	Italian
2002-2003	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2002-2003	Computer Architecture	6	Bachelor	Information Engineering	Italian
2002-2003	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2001-2002	Computer Architecture Laboratory	2	Master	Information Engineering	Italian
2001-2002	Operating Systems and Security	3	Master	Management of Financial Inst.	Italian
2001-2002	Computer Architecture	6	Bachelor	Information Engineering	Italian
2001-2002	Informatics for Industrial Applications	6	Bachelor	Information Engineering	Italian
2001-2002	Database management	3	Bachelor	Management of Financial Inst.	Italian
2000-2001	Advanced Computer Architecture	12	Master	Information Engineering	Italian
2000-2001	Database management	3	Master	Management of Financial Inst.	Italian
2000-2001	Computer Architecture	6	Bachelor	Information Engineering	Italian
1999-2000	Advanced Computer Architecture	12	Master	Information Engineering	Italian
1999-2000	Computer Architecture	6	Bachelor	Information Engineering	Italian

International Teaching

Prof. Giorgi held invited lectures on "Multi-Core and Many-Core architectures" at the University of Tampere, Finland in October 2013.

20 Coordination of Teaching and Research Activities

- 2014-present **co-founder** of the "CompuThink Lab" as a representative of the "Computer Architecture Lab".
- 2001-2009 **Technological Area Coordinator** for Master in New Technologies and Company Management (University of Siena).
- 2007-present **co-responsible** of the "Computer Archicture Lab", with more than 30 workstations, major computing facilities and having equipment and donations from "AMD", "HP-Labs", "Intel", "NVIDIA", "SECO", "ST-Microlectronics", "Xilinx".